VARIABLE DRIVE FOR PRINTHEAD

BACKGROUND OF THE DISCLOSURE

[0001] Thermal inkjet printheads employ drop ejectors which include firing resistors to vaporize fluid in firing chambers, resulting in droplet ejection through nozzles respectively associated with the firing chambers. There has been a trend toward increasing the number of firing chambers and associated resistors on the printhead, leading to increased complexity in driving the firing resistors. In the past, multiple drivers have typically been used to apply the firing signals to different groups of firing resistors. Firing only one resistor at a time by a given driver reduces or prevents energy variation error terms that may occur due to parasitic effects, but at the expense of increased interconnection complexity and performance. For these and other reasons, there is a need for the present invention.

SUMMARY OF THE DISCLOSURE

[0002] A driver for driving simultaneously a variable number of firing resistors for a printhead includes a drive circuit for supplying a drive signal for firing the variable number of firing resistors, and a circuit for adjusting a magnitude of a voltage or current of the drive signal in dependence on the variable number of firing resistors to be fired simultaneously.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Features and advantages of the disclosure will readily be appreciated by persons skilled in the art from the following detailed description when read in conjunction with the drawing wherein:

[0004] FIG. 1 is a simplified schematic block diagram illustrating an embodiment according to the present invention of a printhead and a printhead controller.

[0005] FIG. 2 is a simplified printhead circuit.

[0006] FIG. 3 is a graphical illustration of an embodiment according to the present invention of a fire signal voltage applied as a function of a number of printhead resistors to be fired.

[0007] FIG. 4 is a simplified schematic diagram illustrating an embodiment according to the present invention of a fire driver circuit for the printhead controller circuit of FIG. 1.

[0008] FIG. 5 is a graphical illustration of an exemplary firing pulse as a function of time.

[0009] FIG. 6 is a functional block diagram of an embodiment according to the present invention of an offset generator comprising the exemplary circuit of FIG. 4.

[0010] FIG. 6A is a table of exemplary offset voltages.

[0011] FIG. 7 is a schematic of an exemplary circuit according to the present invention for implementing an offset generator comprising the circuit of FIG. 4.

[0012] FIG. 8 is a schematic circuit diagram of an exemplary circuit according to the present invention for implementing functions of the gate drive and level shift circuit, the dv/dt sense circuit and the gate drive circuit comprising the circuit of FIG. 4.

[0013] FIG. 9 is a simplified schematic block diagram illustrating an alternate embodiment according to the present invention of a printhead and a printhead controller.

DETAILED DESCRIPTION OF THE DISCLOSURE

[0014] In the following detailed description and in the several figures of the drawing, like elements are identified with like reference numerals.

[0015] An embodiment of a printhead firing arrangement is illustrated in simplified form in FIG. 1. An inkjet printhead 50 has a set of firing resistors 60 which are energized to fire droplets of fluid, e.g. ink, from respective firing chambers through respective nozzles, as is known in the art. The printhead 50 in this exemplary embodiment receives a set of control signals and a set of firing pulses from a printhead control 100. The control signals select the particular resistors to be fired during a firing cycle, and the firing pulses are applied to the resistors selected to be fired.

[0016 In this exemplary embodiment, the control signals and the firing pulses are provided by a printhead control circuit 100. The circuit 100 receives the print data which identify the firing pattern for successive firing cycles. This data is converted by control logic 110 into the control signals which are provided to the printhead, and fire control signals provided to a fire drive circuit 130. The print data is also applied to a resistor sum circuit or nozzle counter 120. It is contemplated that a plurality of fire drive circuits may be employed to drive corresponding subsets, typically called "primitives," of the firing resistors. For example, each subset of firing resistors driven by a fire drive circuit may comprise eight firing resistors in one embodiment, sixteen firing resistors in another embodiment, and sixty four firing resistors in yet another embodiment. The particular number of fire drive circuits for a given control circuit 100 will depend on the particular printhead, i.e the number of firing resistors on the printhead, as well as other application-specific parameters. Each fire circuit has an associated resistor sum or counter circuit to determine the number of resistors to be fired in the particular subset during the firing cycle.

[0017] The resistor sum circuit 120 analyzes the print data for a firing cycle to determine how many resistors of the resistors which can be driven by the fire circuit 130 will be fired during the cycle. In an exemplary

embodiment, the circuit 120 is implemented as a bit wise adder. The circuit 120 generates a signal DSUM whose value is indicative of that number of resistors. For example, if the number of resistors which can be driven by the fire circuit 130 is eight, then the DSUM signal value could indicate from 0 resistors to a maximum of 8 resistors for a given firing cycle. The following table describes exemplary outputs for an embodiment wherein the primitive size is eight nozzles.

DSUM Output Decoding

Input	Output
#Resistors to be fired	DSUM
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8

[0018] The exemplary fire circuit 130 receives the fire control signals from the control logic 110 and the DSUM signal from resistor sum 120, and generates a fire pulse during the firing cycle whose voltage magnitude is dependent on the firing data, and particularly varies as a function of the DSUM signal. In an exemplary embodiment, the magnitude of the fire pulse voltage is proportional to the number of resistors to be fired during the cycle, and particularly monotonically increases as the number of resistors to be fired increases.

[0019] Consider the simplified exemplary printhead circuit model shown in FIG. 2. The printhead firing voltage V_{fire} is applied to the printhead firing

resistors 60-1... 60-n through a parasitic resistance 64, a common mode error resistance R_c. Each of the firing resistors is in series with an FET switch whose resistance is depicted as respective resistances 62-1 ... 62-n. The states of the FET switches are controlled by the printhead control signals applied to the printhead. The common mode error resistance acts as a voltage divider with the parallel combination of the firing resistances and FET resistances. The voltage applied to each firing-FET resistor leg, V_{nozzle}, varies based on the number of nozzles being fired, causing the delivered current I_1... I_n, and thus the energy to each fired nozzle to vary. This variation is due to the voltage divider effect resulting from the common mode resistance.

[0020] To compensate for this variation in energy, the magnitude of the firing voltage V_{fire} is varied in dependence on the number of nozzles being fired during a given firing cycle. FIG. 3 graphically illustrates this variation as a function of the number of nozzles fired for an exemplary embodiment. V_{fire} increases monotonically as the number of nozzles being fired increases, such that the voltage applied to each nozzle V_{nozzle} remains substantially constant. VP is the supply voltage for the fire drive circuit, and also is constant.

[0021] In another embodiment, a current characteristic of the resistor drive signal can be controlled in dependence on the number of nozzles being fired in a given firing cycle, instead of a voltage characteristic as described above. In such an alternate embodiment, the magnitude of the current I_{fire} is increased as the number of nozzles being fired simultaneously during the cycle increased.

[0022] An embodiment of a fire drive circuit 130 is schematically shown in FIG. 4. At the output side of the circuit are two FET transistors 132, 134 connected in series between a voltage node VP and ground. The fire voltage V_{fire} is developed at node 133 between the two FETs, at a variable offset voltage below VP. The variable offset voltage is set by an offset generator 140, which sets the offset voltage value ΔV in dependence on the

value DSUM, i.e. the number of resistors to be fired during a given firing cycle. The gate drive on FET 132 is set by a gate drive and level shift circuit 150, in response to the firing data, the value ΔV, and a signal from a dv/dt sense circuit 160. The gate drive on FET 134 is set by a gate drive circuit 170, in response to the fire control signal and the signal from circuit 160.

[0023] The gate drive circuit 150 functions to set the fire voltage pulse maximum value to the offset voltage level set by the offset generator 140, by setting an appropriate drive on the high side FET 132, and also provide proper pulse turn on shaping. FIG. 5 illustrates an exemplary fire voltage pulse, with the gate drive circuit 150 setting the ramp up to the voltage set by the offset generator. The dV/dt sense circuit 160 functions to control the ramp up characteristic, and, with the gate drive circuit 170 and FET 134, to pull down the voltage at the node 133 at the end of the pulse, in response to the fire control signal from circuit 110 (Fig. 1). Thus, the circuit 160 sets the ramp down slope at the end of the firing pulse.

[0024] FIG. 6 is a functional block diagram of the programmable offset generator 140. There is a fixed offset voltage provided by fixed offset 140A, and a data variable offset voltage (DSUM offset) provided by a variable offset 140B which is dependent on DSUM. FIG. 6A shows a table of exemplary offset voltages from VP, for a case wherein the fire drive circuit fires up to eight nozzles, wherein the offset voltages are rounded to the nearest .1 volt. The fixed offset is 1.0 volt for this example. In this embodiment, the output of the offset generator 140 is a voltage value ΔV = VP-Fixed Offset Voltage - DSUM offset voltage.

[0025] FIG. 7 is a schematic of an exemplary circuit for implementing the offset generator 140. Other circuit arrangements could alternatively be employed. The circuit of FIG. 7 implements a digital to analog conversion function, converting a digital value (DSUM) into a corresponding voltage. The circuit 140 includes a resistor 140-1 and an FET 140-2 connected in series between voltage VP and ground. A current mirror circuit comprising a temperature stabilized reference voltage V_{REF}, with a resistor 140-3 and an

FET 140-4 connected in series between the reference voltage and ground. The reference current drives the gates of transistors 140-2, 140-5, 140-6, 140-7 and 140-8. The sizes of the junctions of FETS 140-5 to 140-8 differ, with transistor 140-5 having a size x, 140-6 a size 2x, 140-7a size 4x and 140-8 a size 8x. Thus, transistor 140-6 conducts twice the current of 140-5 in the on state, transistor 140-7 four times the current of 140-5 in the on state, and transistor 140-8 eight times the current of 140-5 in the on state. The output of the circuit 140 is taken at node 140-20. Each of transistors 140-5 to 140-8 is connected between ground to node 140-20 through a corresponding transistor switch 140-9 to 140-12. The gates of each transistor switch are driven by an output of decoder 140-13, which decodes DSUM when enabled by an enable signal (ENABLE_ΔV_ADJ) into corresponding on or off states at outputs 140-14 to 140-17. The decoder outputs turn on selected ones of the switches 140-9 to 140-12 in dependence on the value of DSUM, which in turn connects node 140-20 to current mirrors through the corresponding FETs 140-5 to 140-8. This will increase the current drawn through resistor 140-1 and the corresponding offset voltage, ΔV.

[0026] FIG. 8 is a schematic circuit diagram of an exemplary circuit 180 for implementing functions of the gate drive and level shift circuit 150, the dv/dt sense circuit 160 and the gate drive circuit 170 of FIG. 4. In this circuit arrangement, transistors Q1 and Q2 are connected to transfer the offset voltage ΔV to an input of the driver operational amplifier O_1. Capacitor C1 and current I1 control the rising edge dV/dt of the firing pulse. Current I3 and capacitor C2 control the falling edge dV/dt. The amplifier O1 actively controls the gate of FET 132 to deliver the desired output voltage (ΔV) and dV/dt characteristic. FET Q3 turns on/off the high state driver 132, in response to the firing data. FET Q4 turns on/off the low side driver 134 in response to the firing data. Other circuit arrangements could alternatively be employed.

[0027] In another embodiment, the pulse width of the firing pulse is dependent on the number of nozzles being fired, as described in U.S. 5,677,577, as well as the magnitude of the firing voltage V_{fire}. FIG. 9 illustrates an embodiment of a printhead control 100' which drives the printhead with firing pulses of variable pulse width and variable voltage. In this case, the control logic 110' is responsive to the print data, and generates a "trigger fire" signal to initiate the start of a printhead firing cycle, as well as the control signals for the printhead. As in the embodiment of printhead control 100 (FIG. 1), the print data is also applied to the resistor sum circuit 120. The resistor sum circuit 120 analyzes the print data for a firing cycle to determine how many resistors of the resistors which can be driven by the fire circuit 130 will be fired during the cycle.

[0028] The printhead control 100' further includes a pulse width adjust circuit function 112, and a fire timer circuit 114. The pulse width adjust circuit 112 converts the DSUM signal into a fire pulse width signal which determines the width of the firing pulses to be provided to the printhead by the fire drive circuit 130. The circuit 112 can in an exemplary embodiment provide a look up table conversion function, whereby the DSUM signal value provides an address for a corresponding fire pulse width value. In general, the more resistors are fired in a given firing cycle, the longer the pulse width.

[0029] The fire timer circuit 114 is responsive to the trigger fire signal and the fire pulse width signal to generate the fire control signal to the fire drive circuit 130. Thus, the start of the firing pulses is triggered by the control logic 110', and the length of the pulses is set by the fire timer 114. In an exemplary embodiment, the fire timer circuit 114 can include a state machine, although other implementations can alternatively be employed.

[0030] The exemplary fire circuit 130 receives the trigger fire signals from the control logic 110 and the DSUM signal from resistor sum 120, and generates a fire pulse during the firing cycle whose voltage magnitude and pulse width are dependent on the firing data, and particularly vary as a function of the DSUM signal. In an exemplary embodiment, the magnitude

of the fire pulse voltage is proportional to the number of resistors to be fired during the cycle, and particularly monotonically increases as the number of resistors to be fired increases. The pulse width monotonically increases as the number of resistors to be fired increases.

[0031] The embodiment of FIG. 9 allows flexibility in the magnitude of the variable firing voltage and the pulse width maximum. By using both variables in an exemplary embodiment, the maximum firing voltage and pulse width can be reduced, in comparison to embodiments in which only variable pulse width or firing voltage is employed.

[0032] Although the foregoing has been a description and illustration of specific embodiments of the invention, various modifications and changes thereto can be made by persons skilled in the art without departing from the scope and spirit of the invention as defined by the following claims.